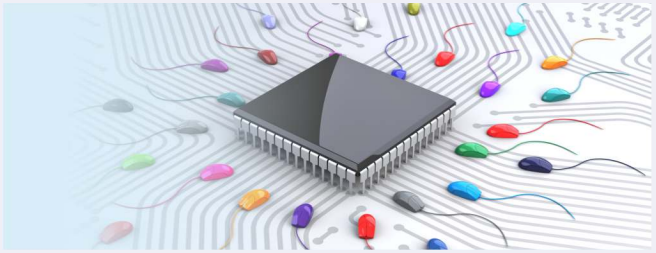
REGISTRATION PROCESS

- Sign up as a participant and complete your details on ATAL portal https://atalacademy.aicte-india.org/login
- Go to FDPs → Select FDP Types VAANI → November (Search for Application No: 2544994561)
- Select the Institute: Krishna Institute of Engineering and Technology (KIET) Deemed to be university, Ghaziabad
- Register for the workshop titled: "**Semiconductor Technology and VLSI Design: Innovation and Emerging Trends**" (Application No: 2544994561).
- Upload the NOC and Apply.



RESOURCE PERSONS

Dr. Neeta Pandey
Professor
Delhi Technological University, Delhi

Dr. Vandana Niranjan
Professor
Indira Gandhi Delhi Technical University for Women (IGDTUW), Delhi

Dr. O.P. Thakur
Scientist-G SSPL
DRDO Delhi

Dr. Abhishek Tomar
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GB Pant University of Agriculture & Technology Pantnagar

Mr. Ankit Rathore
Technical Lead
HCL Technologies

Mr. Varun Bhadana
Sr. Staff Engineer
Renesas, Noida

Mr. Ajay Chopra
Teachnical Lead
HCL Technologies

Dr. Rajendra Pratap
Vice President & General Manager
Vervesemi, Noida

GUIDELINES

- No registration fee.
- All faculty members and research scholars from AICTE-approved institutions or universities, as well as professionals from industry and government, are eligible to participate in the workshop.
- Participants will be selected on first-come first-served basis.
- To get Certificate 80% attendance is mandatory.
- Compulsory feedback in ATAL portal.
- A digital certificate will be issued by the ATAL Academy downloadable from the ATAL portal on successful completion.
- Eligible participants will be issued ATAL Academy Certificate.

ORGANIZING COMMITTEE

CHIEF-PATRON

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Hon'ble Chairman
KIET Deemed to be University

Shri Atul Garg
Chancellor
KIET Deemed to be University

PATRON

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Dr. Adesh Kumar Pandey
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Dr. Vibhav Kumar Sachan
Dean (R&D) & Dean (ECE), and ECE (VLSI D & T)
KIET School of Management

WORKSHOP CO-COORDINATOR

Dr. Shraddha Sood
Assistant Professor, ECE
KIET School of Management

ORGANIZING COMMITTEE

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Dr. Richa Srivastava, ECE
Dr. Urvashi Gupta, ECE
Dr. Shivani Yadav, ECE
Dr. Rashi Choudhary, ECE
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KIET DEEMED TO BE UNIVERSITY
DELHI-NCR, GHAZIABAD, UP (INDIA)
(Under Section 3 of the UGC Act, 1956)
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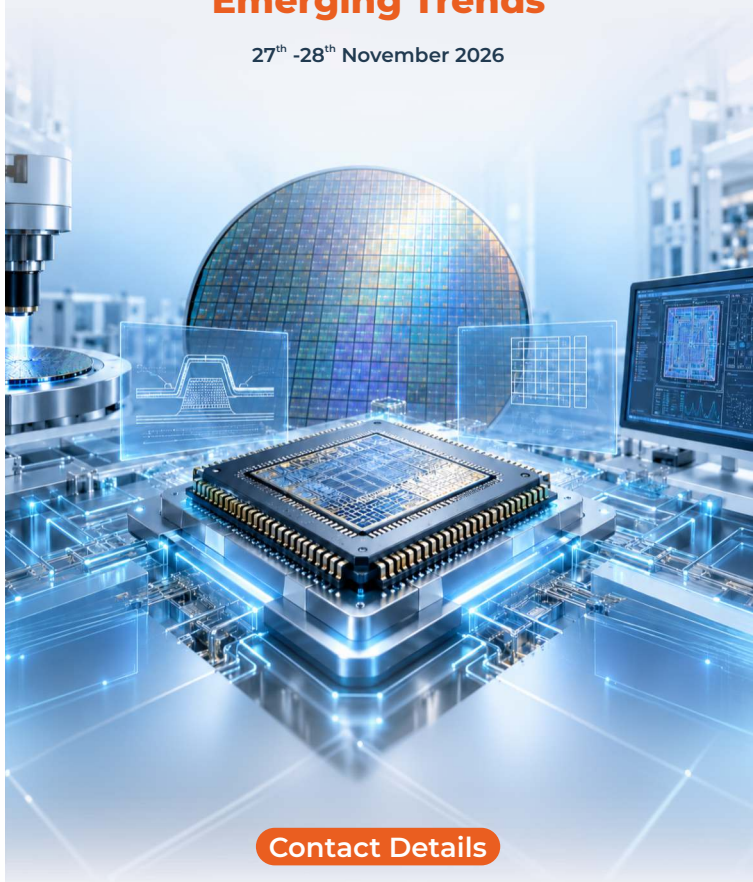
AICTE- Vibrant Advocacy for Advancement and Nurturing of Indian Languages(VAANI)

Two Days Sponsored Workshop

on

Semiconductor Technology & VLSI Design: Innovation and Emerging Trends

27th -28th November 2026



Contact Details

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ABOUT KIET



Established in 1998, KIET is a premier institution known for academic excellence and industry-aligned education. With a 27-year legacy across Engineering, Pharmacy, Management, and Computer Applications, KIET attained Autonomous Status in 2024 and Deemed-to-be-University status in 2025. The Institute has 9300+ students, 440+ faculty members, and provides 100% Placement & Internship assistance. KIET is accredited with NAAC 'A+', with all eligible programs NBA accredited. In NIRF 2025, it secured Rank 71 in Pharmacy, 151–200 band in Engineering, and 11–50 band in Innovation. It also holds the QS I-GAUGE Diamond Rating and DSIR-SIRO recognition. Through TBI-KIET, Innovation Centre, CRPC, Centres of Excellence, and advanced facilities, KIET promotes innovation, research, entrepreneurship, and industry readiness.

ABOUT ECE DEPARTMENT

The Department of ECE nurtures industry-ready, innovative, and socially responsible engineers through experiential learning and holistic development. It builds strong foundations in hardware and software, supported by qualified faculty and industry linkages, while promoting technical excellence, higher studies, research, and entrepreneurship. Key research areas include Optical Integrated Circuits, Signal Processing & Communication, Semiconductor Devices, Advanced Microwave Techniques, and emerging ECE domains. MoUs with Nokia, ISRO, and Texas Instruments strengthen industry–academia collaboration. The department aspires to become a Centre of Excellence, fostering innovation, ethical values, and technology for societal development.

ABOUT VAANI

The AICTE VAANI Workshop promotes inclusive technical education through regional languages, providing a platform to explore emerging technologies, innovative practices, and applications. It fosters knowledge exchange, capacity building, and stronger academia–industry collaboration among faculty, researchers, and students.

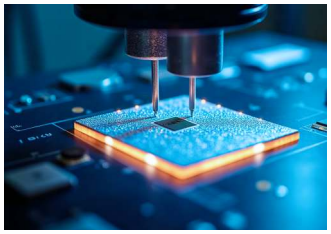
ABOUT WORKSHOP

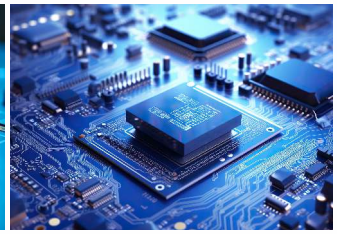
The VAANI Workshop on "**Semiconductor Technology and VLSI Design: Innovation and Emerging Trends**", sponsored by AICTE–ATAL, is a two-day technical workshop aimed at providing participants with contemporary knowledge and practical insights into the rapidly evolving field of semiconductor technology and Very Large-Scale Integration (VLSI) design. The workshop brings together emerging concepts, design methodologies, and industry-relevant practices that are shaping the future of semiconductor and electronic system development.

The sessions will explore critical areas including Challenges in Non-Volatile SRAM Design, Low-Power VLSI Design Techniques, and Wide Band Gap Semiconductor Materials, highlighting their significance in developing energy-efficient and high-performance electronic systems. Participants will also gain insights into Full-Custom Design, covering the journey from conceptualization to IC implementation, along with CDC ASIC Clocking and its role in reliable high-speed digital designs.

The workshop will further address the Physical Design Implementation Flow and the Complete VLSI Design Flow, providing a comprehensive understanding of the stages involved in transforming circuit concepts into manufacturable integrated circuits. A dedicated session on AI-Driven Techniques in VLSI Design will highlight the growing role of artificial intelligence in design automation, optimization, verification, and semiconductor innovation.

The workshop is designed to foster knowledge exchange, industry-oriented learning, research perspectives, and innovation among faculty members, researchers, and students, thereby strengthening their capabilities in emerging semiconductor technologies and next-generation VLSI design.







EXPECTED OUTCOMES

Participants will be able to

- Understand emerging trends and challenges in semiconductor and VLSI technologies.
- Gain insights into low-power, non-volatile memory, and advanced semiconductor materials.
- Understand the complete VLSI design flow, from RTL to physical implementation and tape-out.
- Develop awareness of full-custom IC design, ASIC clocking, and physical design techniques.
- Explore AI/ML applications in VLSI design and optimization.
- Identify opportunities for research, innovation, industry collaboration, and future career development in the semiconductor ecosystem.

Contents of workshop

- **Challenges in Non-Volatile SRAM Design:** Design challenges related to stability, reliability, power consumption, and data retention in next-generation non-volatile SRAM.
- **Low Power VLSI Design Techniques:** Advanced techniques for minimizing dynamic and leakage power while maintaining performance and reliability in VLSI circuits.
- Wide Band Gap Semiconductor Materials: Materials such as GaN and SiC, their superior properties, and applications in high-power, high-frequency, and high-temperature electronics.
- **Full Custom Design:** Idea to IC Implementation: The complete full-custom design process, from circuit concept and schematic development to layout, verification, and IC fabrication.
- **CDC ASIC Clocking:** Clock-domain crossing challenges and robust clocking techniques for reliable and high-performance ASIC designs.
- **Physical Design Implementation Flow:** Physical implementation process including floorplanning, placement, clock-tree synthesis, routing, and design-rule verification.
- **Complete VLSI Design Flow:** Overview of end-to-end VLSI flow from RTL design and synthesis to physical design.
- **AI-Driven Techniques in VLSI Design:** Application of Artificial Intelligence and Machine Learning for design optimization, verification, automation, and improved chip performance.